IN THE CLAIMS

Please amend the claims as follows:

Claims 1-23 (Canceled)

24. (new) A method, comprising:

receiving, by a network adapter, a security association (SA) and a first integrity indicator, said SA and first integrity indicator being generated by an information handling apparatus (IHA);

generating, by said network adapter, a second integrity indicator based on said SA; and

verifying, by said network adapter, that said SA within said network adapter is substantially similar the SA generated by said IHA by comparing said first integrity indicator to said second integrity indicator.

25. (new) The method of claim 24, further comprising:

generating, by said IHA, said first integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

26. (new) The method of claim 24, further comprising:

generating, by said network adapter, said second integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

27. (new) The method of claim 24, further comprising:

indicating, by said network adapter, the integrity of said SA to said IHA.

28. (new) The method of claim 24, further comprising:

setting an integrity error bit in a memory in the IHA.

29. (new) An apparatus, comprising:

a network adapter comprising an integrated circuit, said integrated circuit is capable of receiving a security association (SA) and a first integrity indicator, said SA and first integrity indicator being generated by an information handling apparatus (IHA), said integrated circuit being further capable of generating a second integrity indicator based on said SA, said integrated circuit being further capable of verifying that said SA received by said integrated circuit is substantially similar the SA generated by said IHA by comparing said first integrity indicator to said second integrity indicator.

30. (new) The apparatus of claim 29, wherein:

said IHA being capable of generating said first integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

31. (new) The apparatus of claim 29, wherein:

said integrated circuit being further capable of generating said second integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

32. (new) The apparatus of claim 29, wherein:

said integrated circuit being further capable of indicating the integrity of said SA to said IHA.

33. (new) The apparatus of claim 29, wherein:

said integrated circuit being further capable of setting an integrity error bit in a memory in the IHA.

34. (new) An article comprising:

a storage medium storing instructions that when executed by a machine result in the following operations:

receiving, by a network adapter, a security association (SA) and a first integrity indicator, said SA and first integrity indicator being generated by an information handling apparatus (IHA);

generating, by said network adapter, a second integrity indicator based on said SA; and

verifying, by said network adapter, that said SA within said network adapter is substantially similar the SA generated by said IHA by comparing said first integrity indicator to said second integrity indicator.

35. (new) The article of claim 34, wherein said instructions that when executed by said machine result in the following additional operations:

generating, by said IHA, said first integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

36. (new) The article of claim 34, wherein said instructions that when executed by said machine result in the following additional operations:

generating, by said network adapter, said second integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

37. (new) The article of claim 34, wherein said instructions that when executed by said machine result in the following additional operations:

indicating, by said network adapter, the integrity of said SA to said IHA.

38. (new) The article of claim 34, wherein said instructions that when executed by said machine result in the following additional operations:

setting an integrity error bit in a memory in the IHA.

39. (new) A system, comprising:

at least one network adapter being capable of being coupled to an information handling apparatus (IHA) via a bus, said network adapter comprising an integrated circuit capable of receiving a security association (SA) and a first integrity indicator, said SA and first integrity indicator being generated by said IHA, said integrated circuit being further capable of generating a second integrity indicator based on said SA, said integrated circuit being further capable of verifying that said SA received by said integrated circuit is substantially similar the SA generated by said IHA by comparing said first integrity indicator to said second integrity indicator.

40. (new) The system of claim 39, wherein:

said IHA being capable of generating said first integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

41. (new) The system of claim 39, wherein:

said integrated circuit being further capable of generating said second integrity indicator based on said SA using a data checking integrity method selected from the group consisting of: checksum, cyclical redundancy checking, Huffman coding, parity checking and has computations.

42. (new) The system of claim 39, wherein:

said integrated circuit being further capable of indicating the integrity of said SA to said IHA.

43. (new) The system of claim 39, wherein:

said integrated circuit being further capable of setting an integrity error bit in a memory in the IHA.